Si TECHNOLOGY ROADMAP FOR UBIQUITOUS COMPUTING, SENSING, AND PERCEPTION

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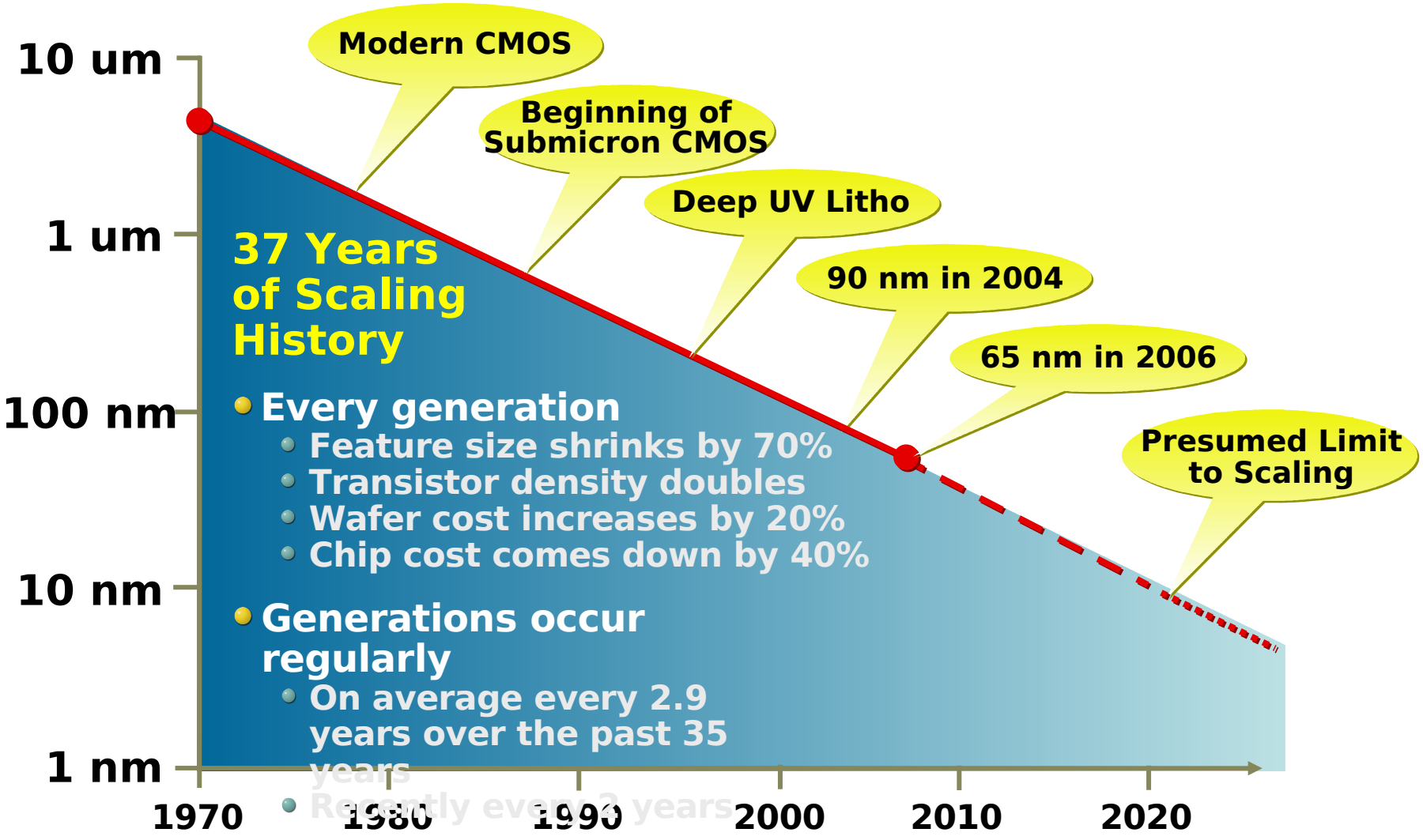
Si TECHNOLOGY ROADMAP FOR UBIQUITOUS COMPUTING

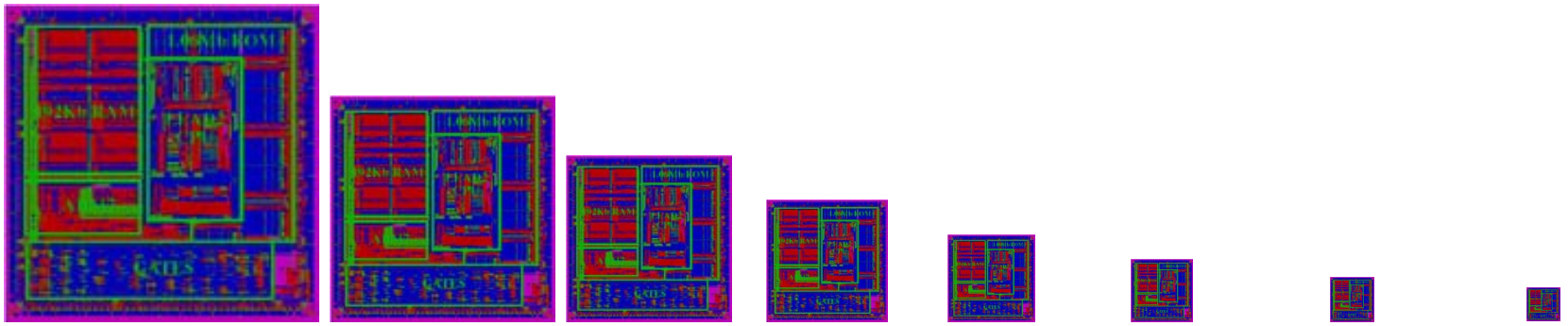
AGENDA

- ►Moore’s Law Scaling
- Design for Low Power
- SOC Integration of Analog/RF Functions
- Digital Radio Processor
- Integrated MEMS
- Conclusion

Semi-Conductor Scaling



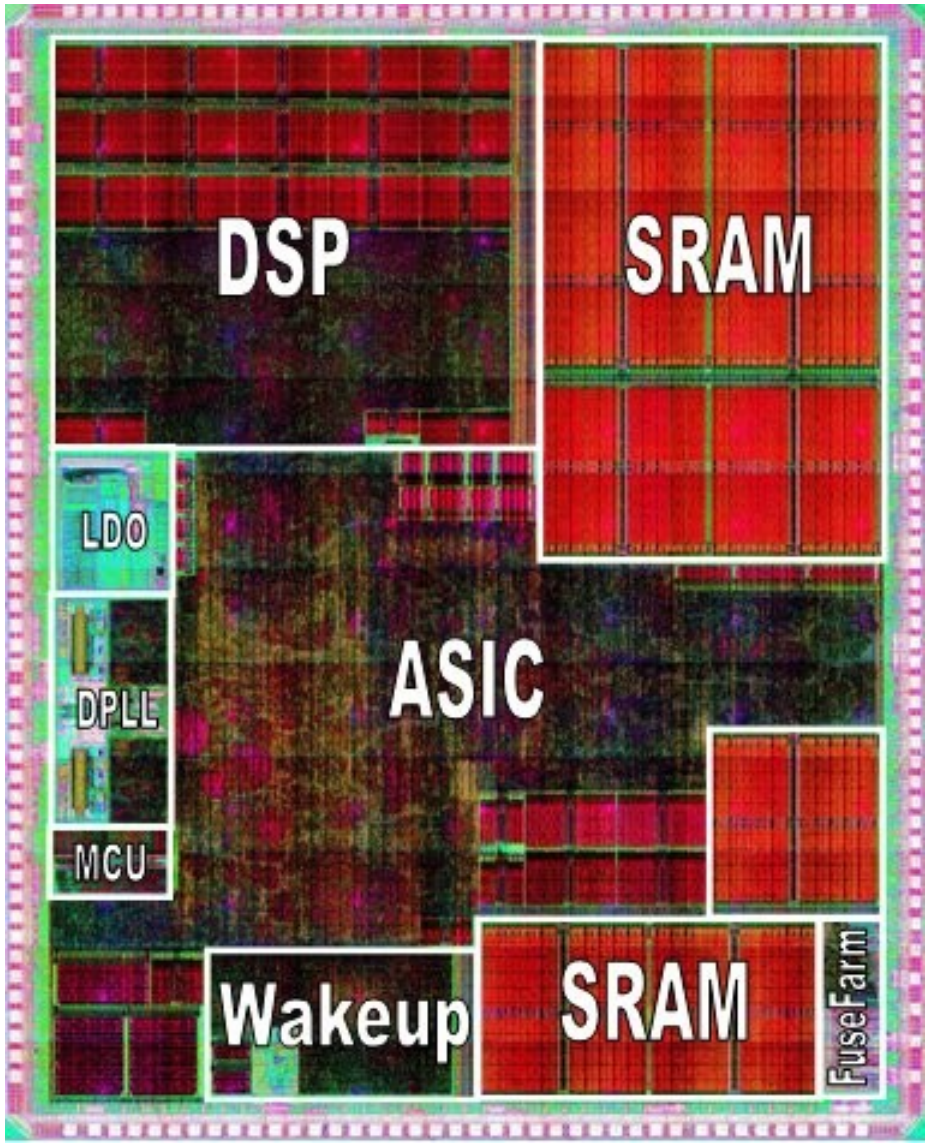
GSM Digital Baseband Evolution



Year	1994	1997	1999	2000	2002	2004	2006	2008
Nano-meter	500nm	350nm	250nm	180nm	130nm	90nm	65nm	45nm
Wafer size	6"	8"	8"	12"	12"	12"	12"	12"
Die size (mm^2)	80.7	46.6	19.2	10.7	6.7	4.2	2.4	1.4
Dies per wafer	310	950	2550	4700	12,200	18,700	26,500	46,500

150X increase in die per wafer

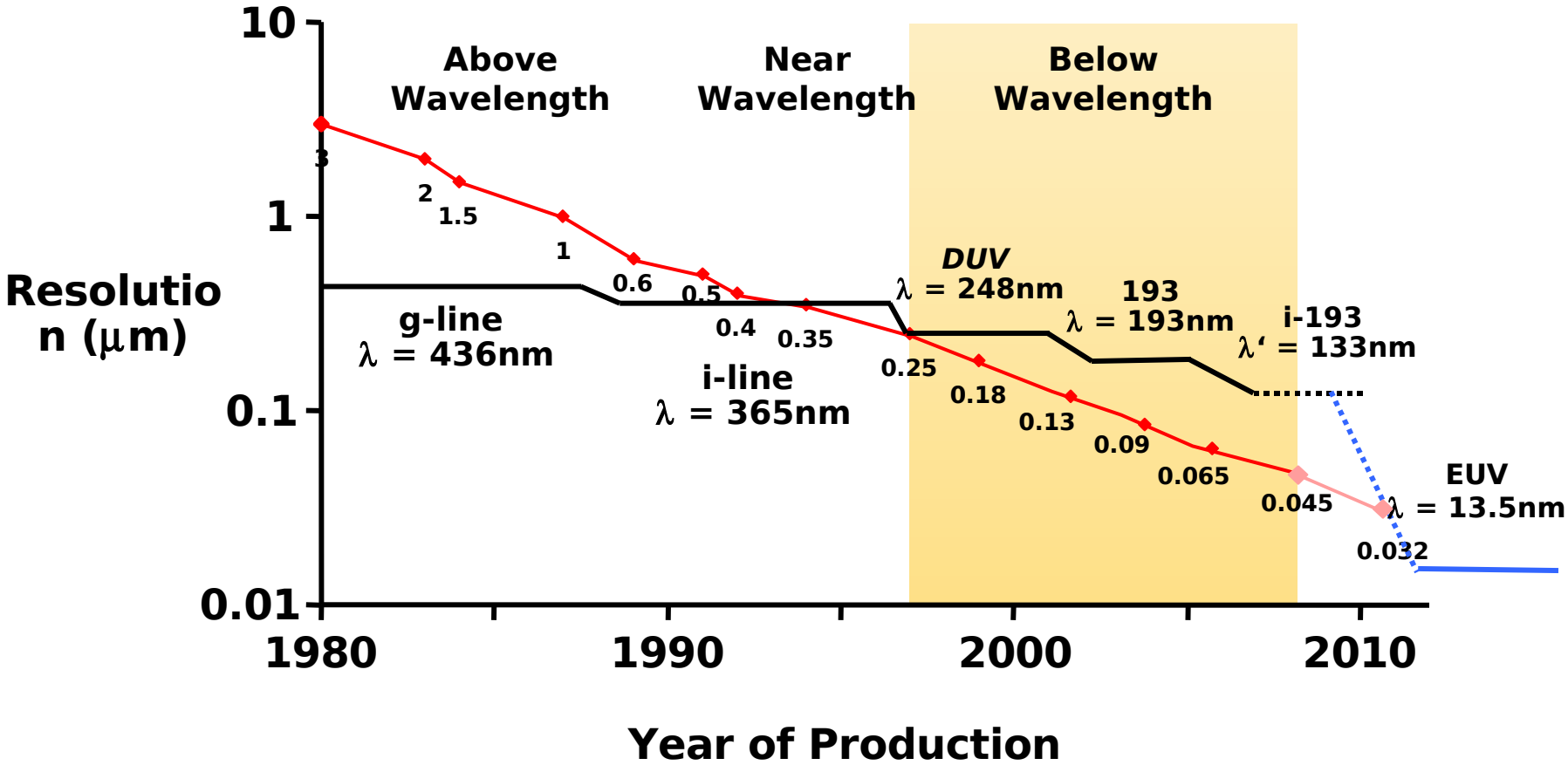
Typical 65 nm Product: DBB chip



Features:

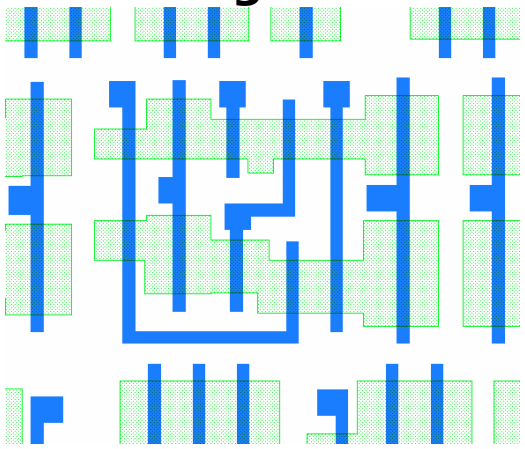
- **Die Size: 13.3mm²**
- **5.9M bits SRAM**
- **1.9M gates of logic**
  - eFuse (dieID) and repair
  - ARM7 uC
  - LEAD3 DSP (250K gates)
  - MegaCell (300K gates)
  - ASIC gates (1.3M gates)
- **Volume Production**

Lithography

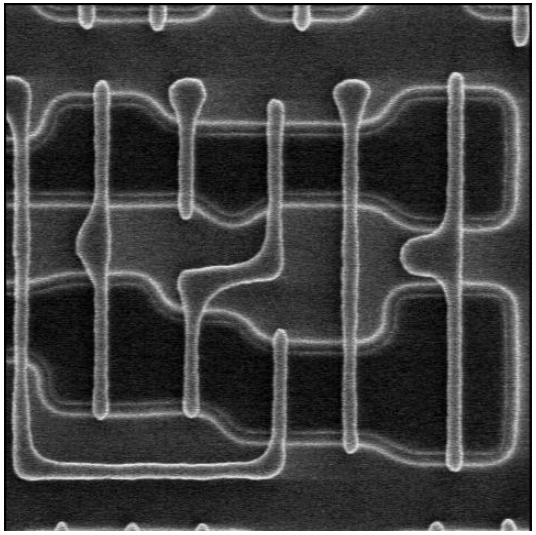


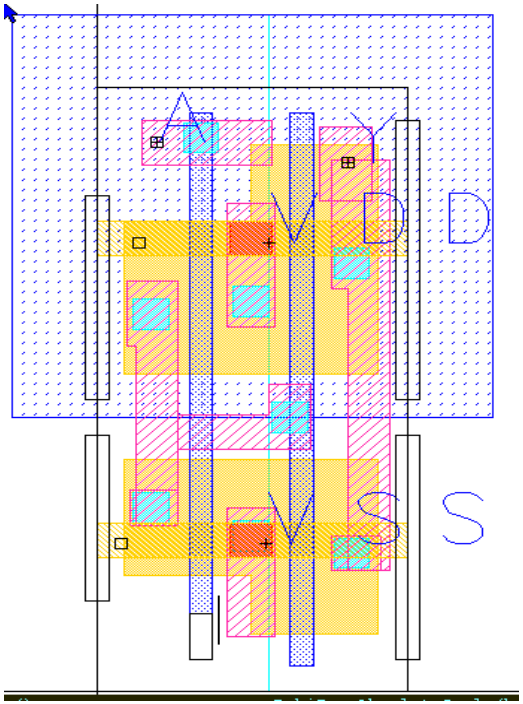
STRUCTURED LAYOUT (45 nm)

Design Data



Silicon





- Vertical poly gates only
- GHOST Poly
- Poly not required to overlap contact
- Max Xstor width change within ACTIVE

Si Technology Roadmap Issues/Trends

- Design for Manufacturing Variations
- Analog/RF & MEMS SOC Integration
- Co-Development of Process, Design Techniques and Architecture
- CMOS processes customized to the application
- Relentless focus on power reduction.

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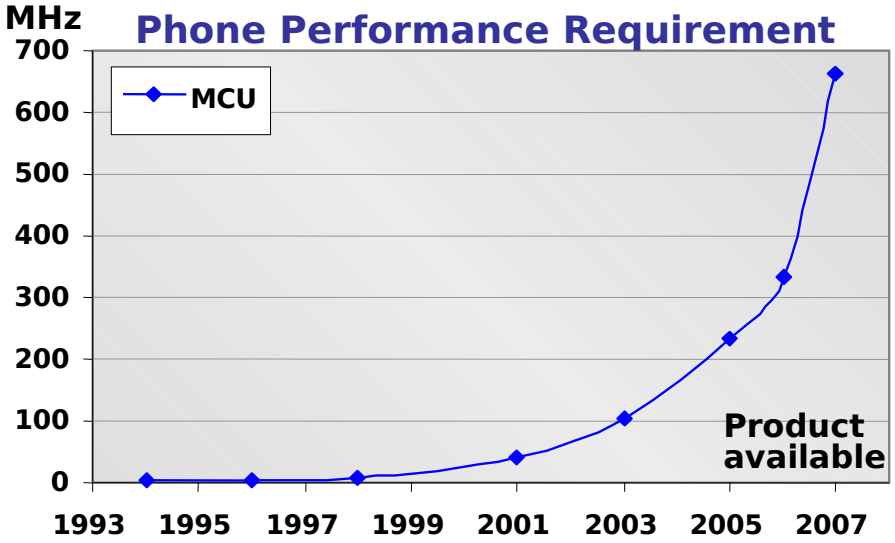
Deep Submicron Processes Demand Enhanced Power Management

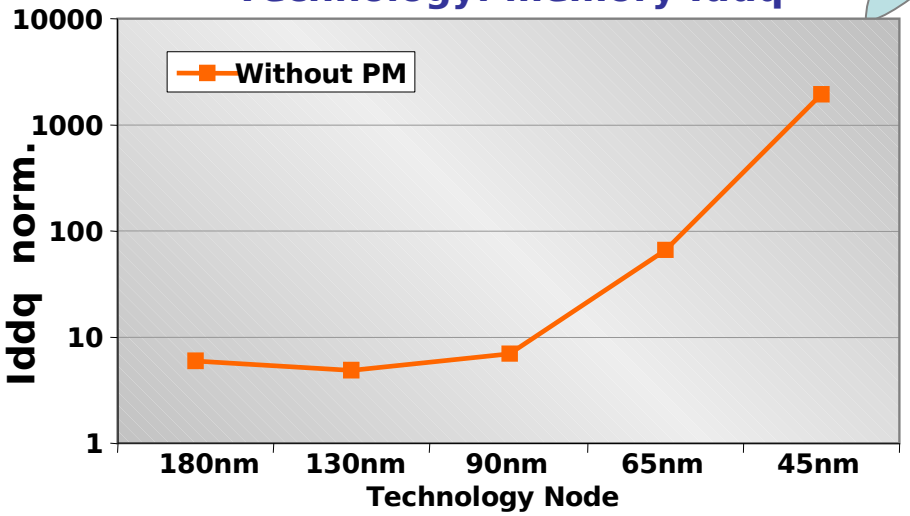


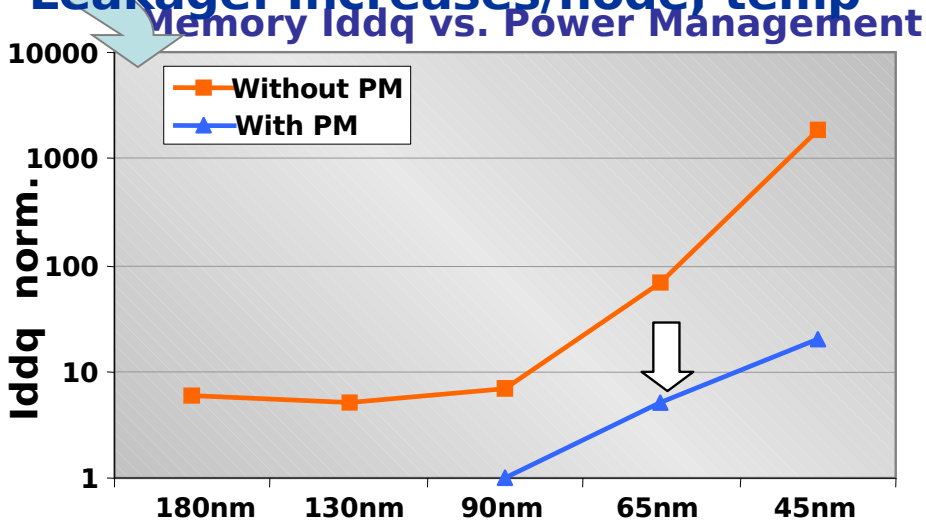
Talk Time: Pwr_Active = CV^2F + Leakage

- C: Decrease/node,offset by complexity
- F: Increases/node
- Leakage: Increases/node, temp.

Standby Time: Pwr_Idle = Leakage

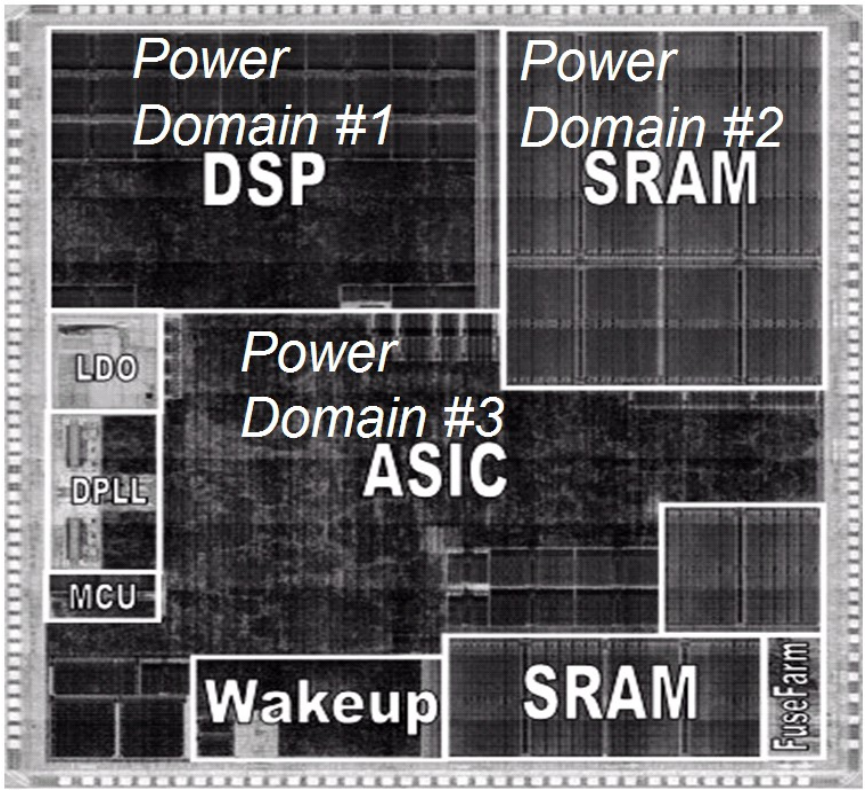
- Leakage: Increases/node, temp



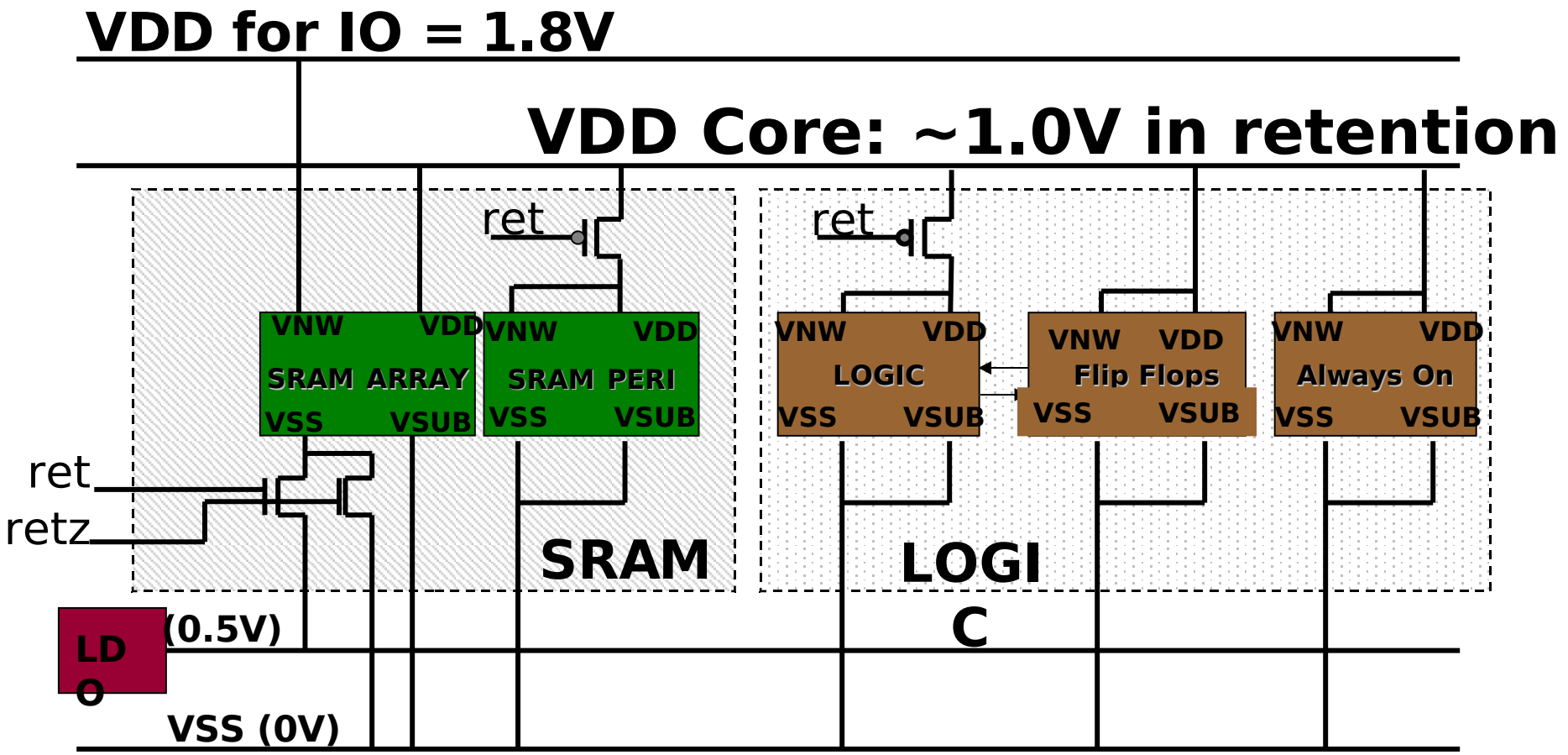


Power Domain Partitioning

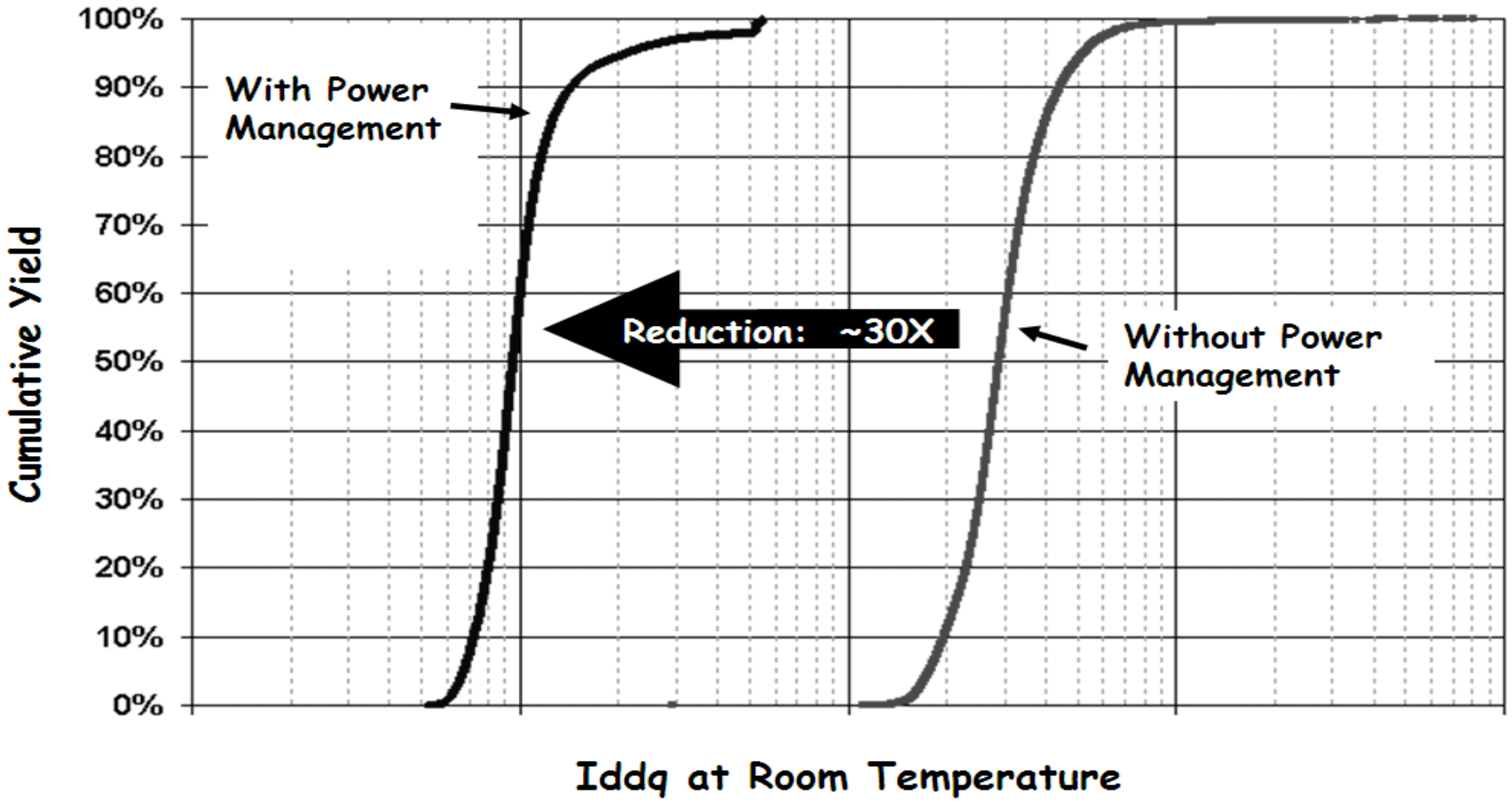
- **Main Power Domains**
  - **DSP**
  - **Data Memory**
  - **Modem Logic**
- **Others**
  - **Power Mngmt Control**
  - **MCU**
  - **DPLL**
  - **Analog**
  - **IO**



Approaches to Power Reduction



Silicon Measurements



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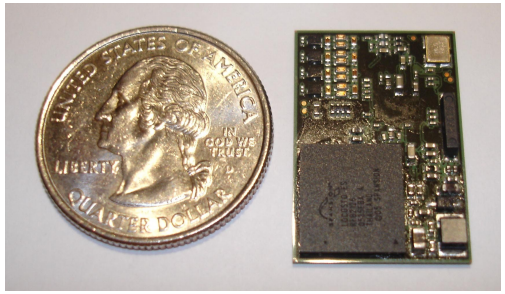
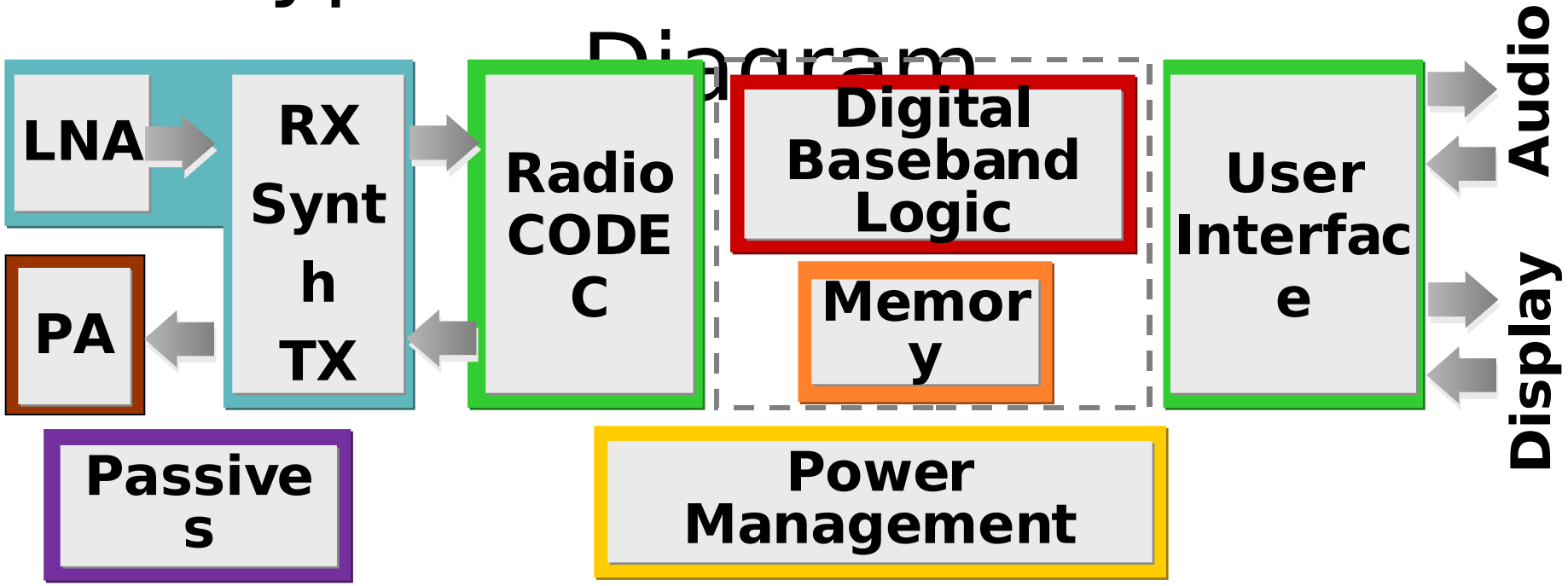
Why Single-Chip Phone?

- "Integration is like gravity”
  - Already happened in hard-disk drives, ADSL, etc
  - Not a single example of reversal
- “$20 phones”
- Large untapped market in India and China
- More “real estate” space for advanced features
- Better reliability
  - Today, more than half of the total components on a board are analog RF components
- Longer talk time




Old Platform

Typical Cell-Phone Block Diagram

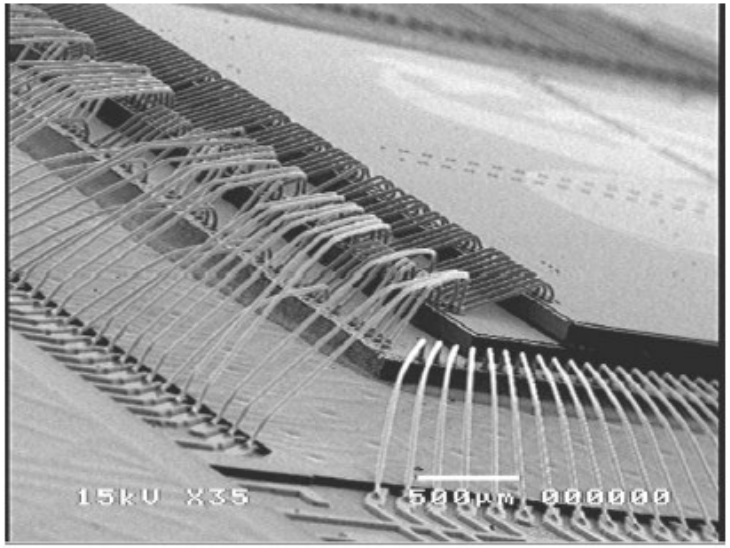


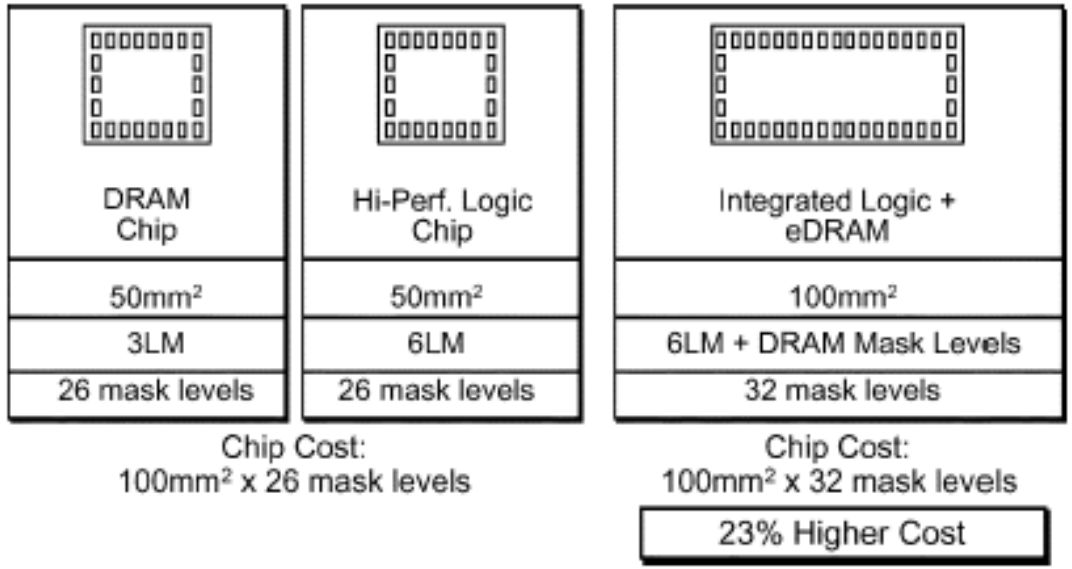
SiGe BICMOS
Discrete Passives (SAW Filters, etc.)
High voltage Analog CMOS
High-power (typically GaAs)
DSM Digital
FLASH EEPROM

Area and cost must be reduced → integrate !

What about SiP Integration?

- Monolithic integration of DRAM would result in significant cost increase due to the need for additional mask levels.
- Memory modules are highly reusable so modularity makes sense.
- No yield impact issue due to in-package





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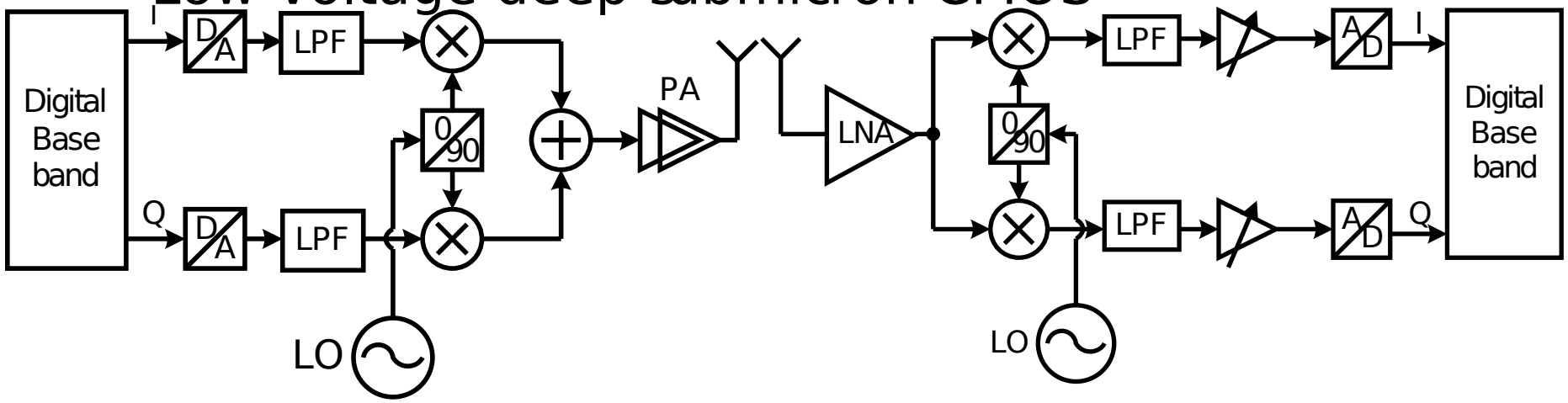
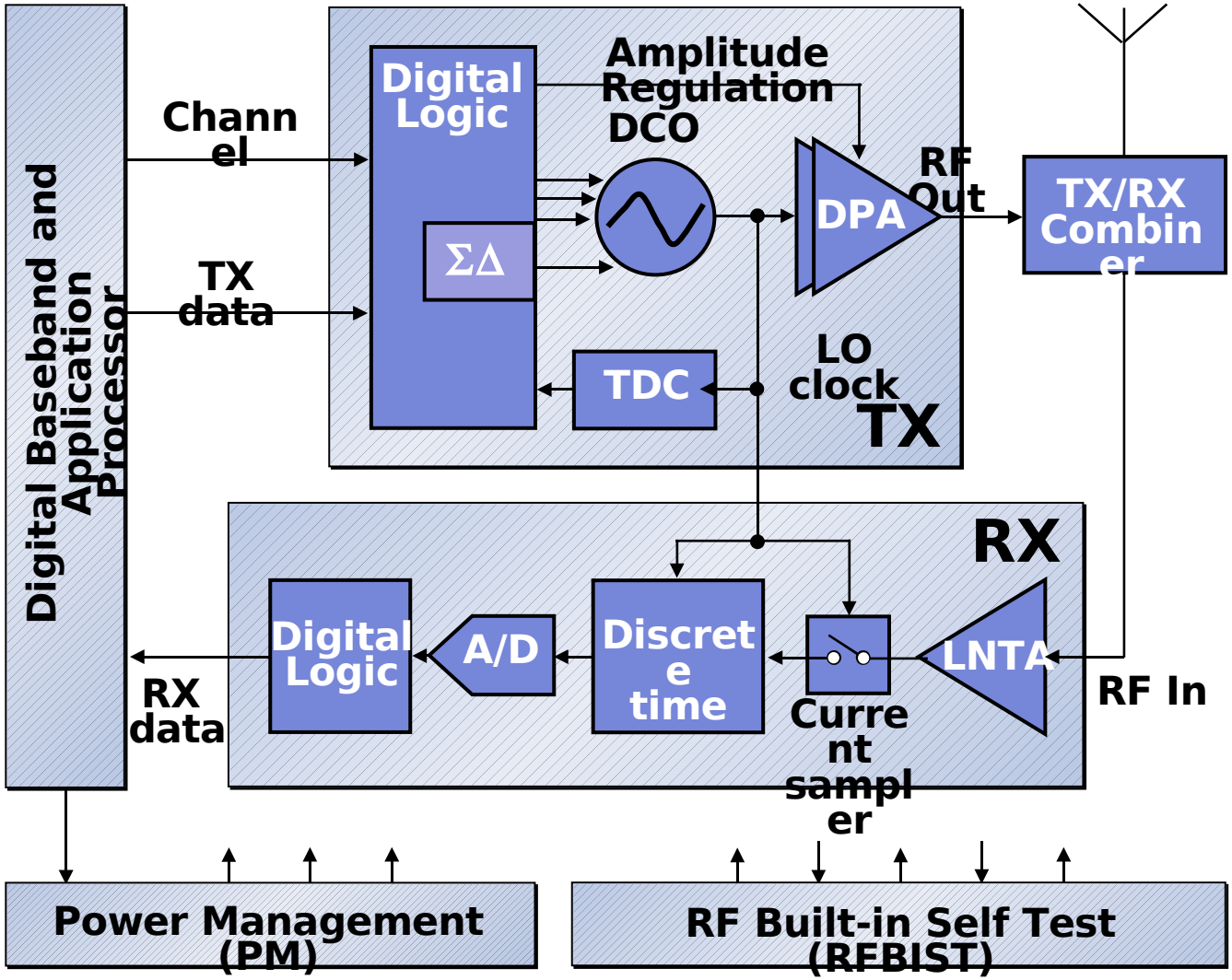
Conventional Transceivers

- RF transmitters in commercial wireless applications are traditionally based on charge-pump PLL's and IQ upconversion mixers
- RF receivers use continuous-time mixing, filtering and amplification
- Design flow and circuit techniques are analog intensive
- Technology incompatible with modern digital processors
  - Low-voltage deep-submicron CMOS



DRP RF Architecture



0.2, 1.25, 2.5,5,
10, 15, 20MHz BW

450, 800, 900,
1800, 1900, 2100,
2500, 3400MHz
Transmission bands

GMSK, QPSK,
8-PSK, 16QAM,
64QAM Modulation

TDMA, FDMA,
CDMA, OFDMA,
IFDMA schemes

Looks like SDR!!

DRP/SoC Proven in Many Products

1/2 the silicon

1/2 the power

1/2 the board area

BlueLink™ Bluetooth

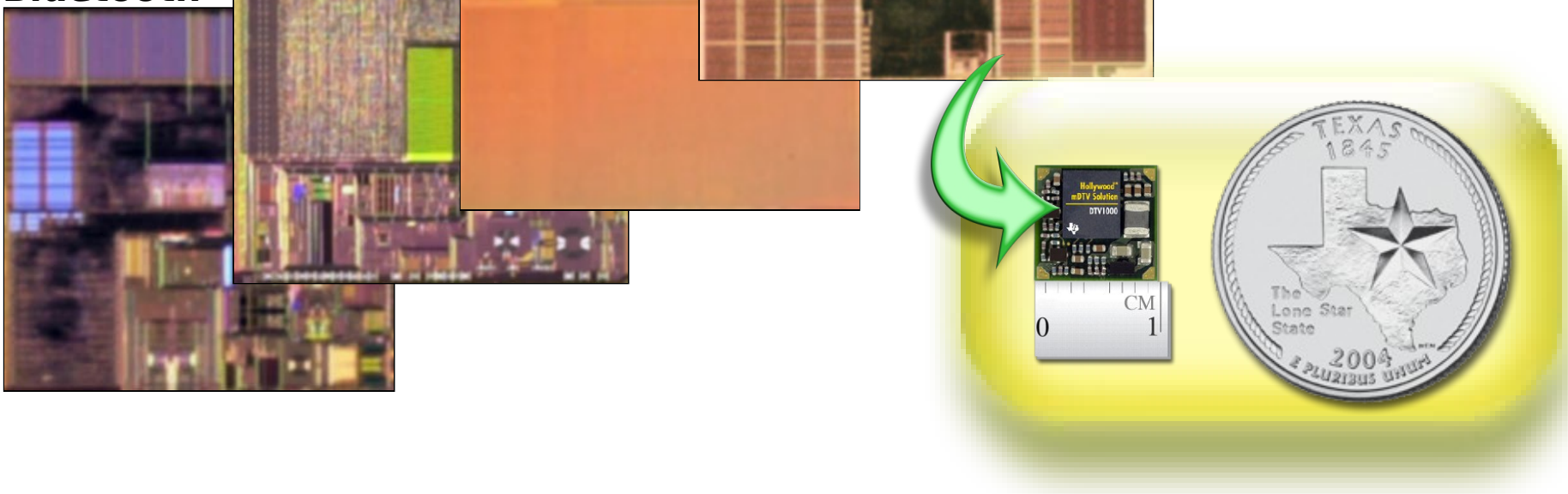
NaviLink™ A-GPS

WiLink™ Wi-Fi

Hollywood™ mDTV

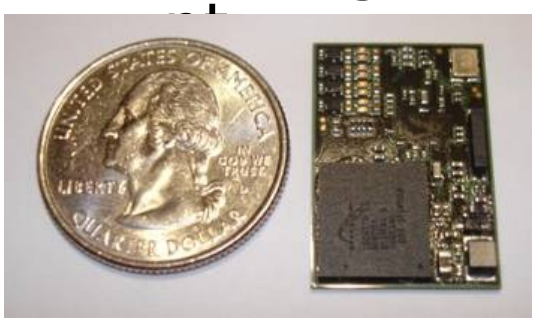
“LoCosto” GSM/GPRS

More to come..



Single-Chip GSM Radio

- 90 nm CMOS
- All-digital PLL
- All-digital TX
- Digitally-intensive RX
- w/o
  - 2-W PA
  - Battery manageme

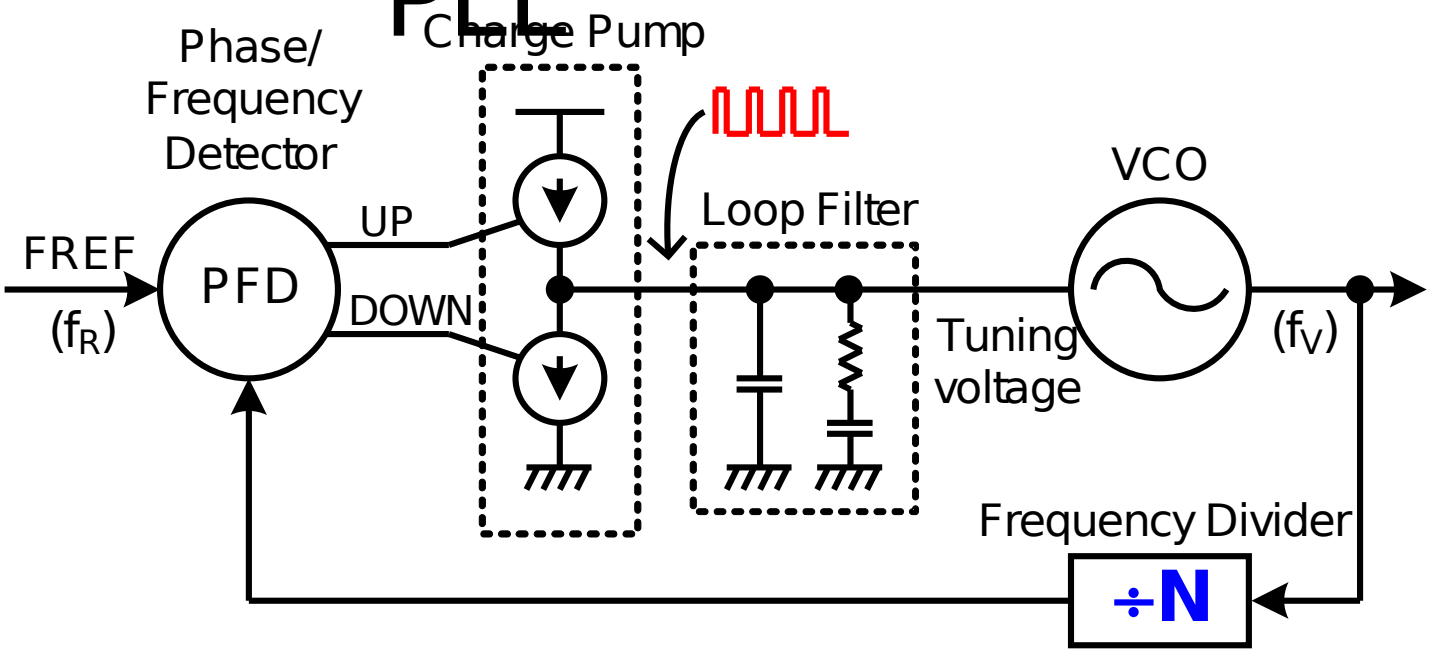


New Paradigm

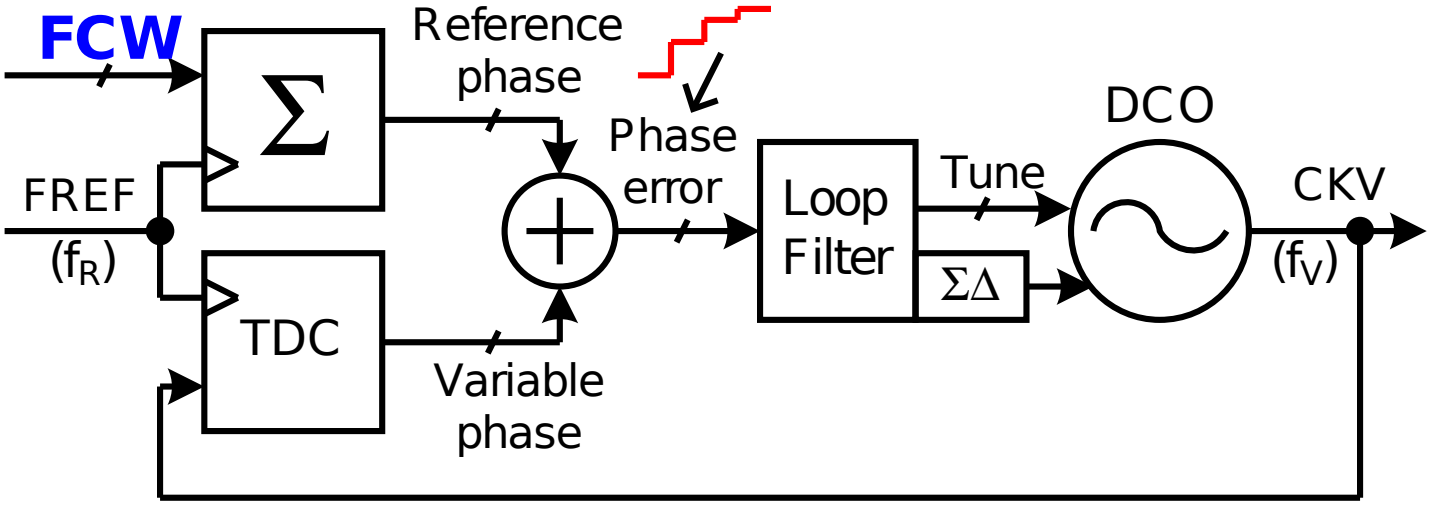
In a deep-submicron CMOS process, time-domain resolution of a digital signal edge transition is superior to voltage resolution of an analog signal

All-Digital PLL vs. Charge-pump PLL

- Charge-pump PLL:
- Suffers from reference spurs
- Tradeoff: bandwidth against spur level



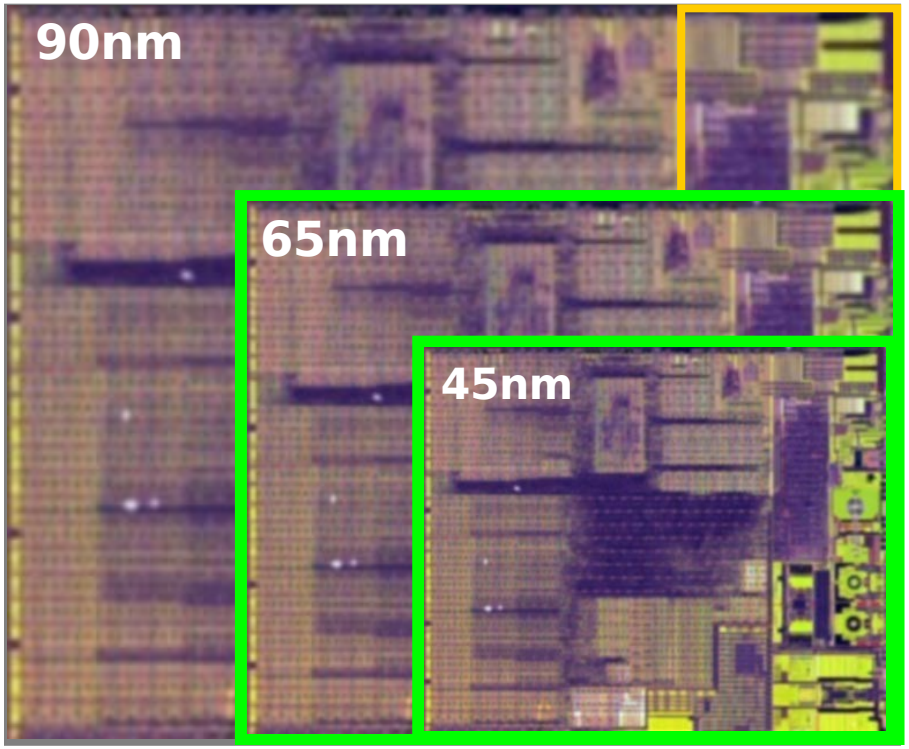
- All-digital PLL:
- True phase domain operation
- Exploits **time resolution** of TDC and DCO



Deep-Submicron CMOS Rules

- **Exploit:**
  - Fast switching characteristics of MOS transistors
  - Small device geometries and precise device matching
  - High density of digital logic: 250 kgates/mm^2 in 90-nm CMOS
  - High density of SRAM memory: 1 Mbits / mm^2 in 90-nm CMOS
- **Avoid:**
  - Biasing currents for analog circuits
  - Reliance on voltage resolution
  - Nonstandard devices not needed for memory and digital logic

SoC Drives Cost Reduction



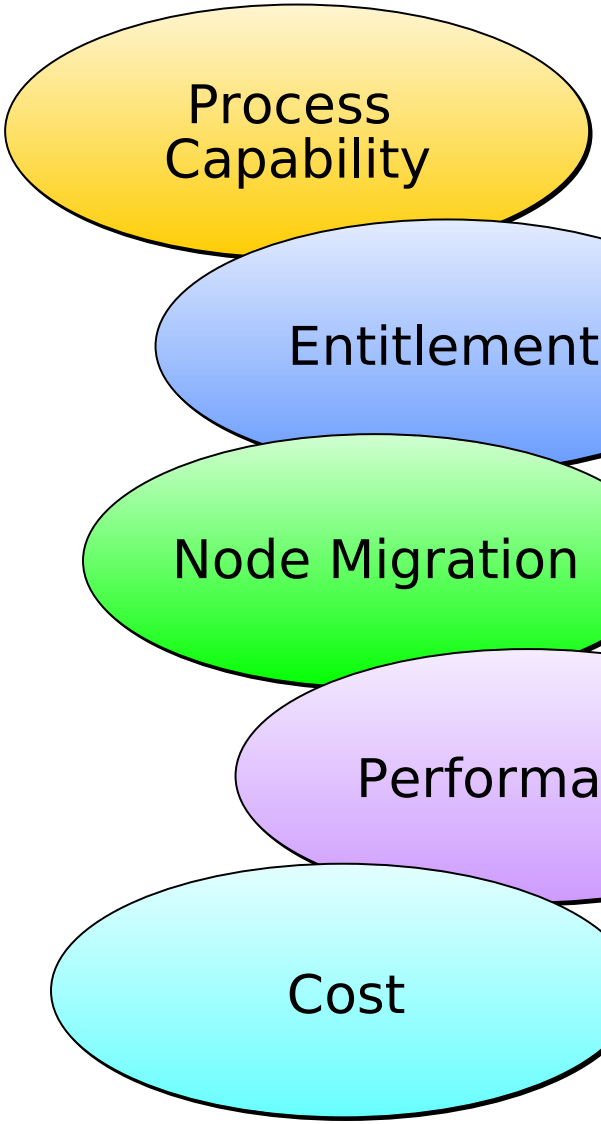
- SoC Integration Includes:
  - Digital baseband
  - SRAM
  - Power management
  - Analog
  - RF
  - Processors & Software

- The DRP technology enables digital implementation of traditional analog RF functions in standard CMOS

- Most advanced process technology used to maximize integration while minimizing cost
  - 90nm (shipping)
  - 65nm (mature design)
  - 45nm and beyond (preliminary)

Digital Radios Offer Many Benefits

Why Digital?



- **We can now clock systems at radio frequencies**
- **Digital technology takes advantage of advanced logic capability (and leverages the wafer process technology investment)**
- **Digital systems scale with lithography and are easy to migrate**
- **Performance improves with new technology, the job keeps getting easier**
- **Digital radios offer excellent performance, low power consumption, high manufacturing yield, and low cost**

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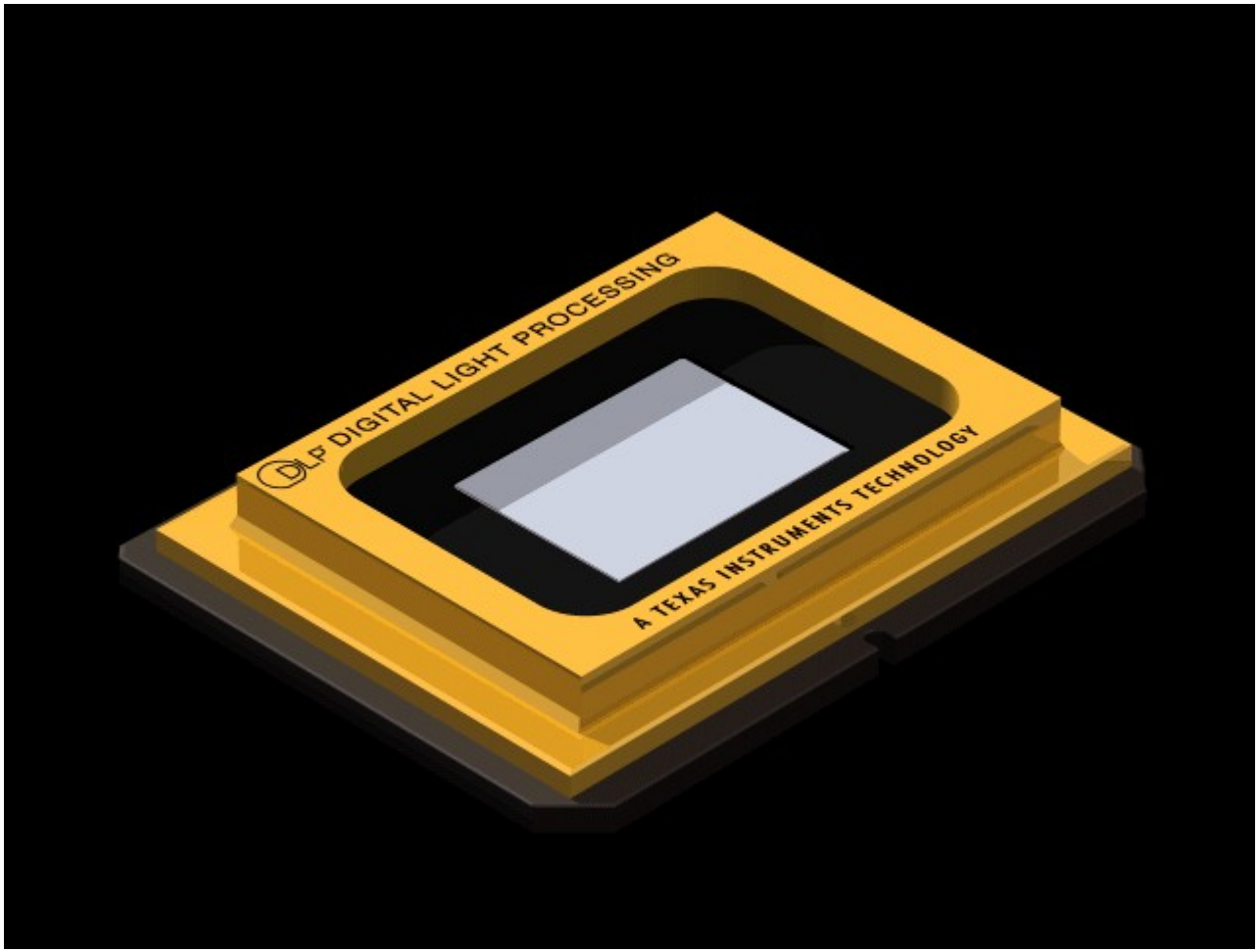
MEMS Integration

- MEMS Integration will also enable products for ubiquitous computing, sensing and perception
  - accelerometers
  - pressure sensors
  - rate gyros
  - integrated microphones
  - resonators
  - RF switches and tuneable capacitors
  - optical switches and phase modulators,
  - micro-fluidic pumps and valves
  - displays
- The Digital Mirror Device (DMD) is an example of integrated MEMS

How the DMD Works



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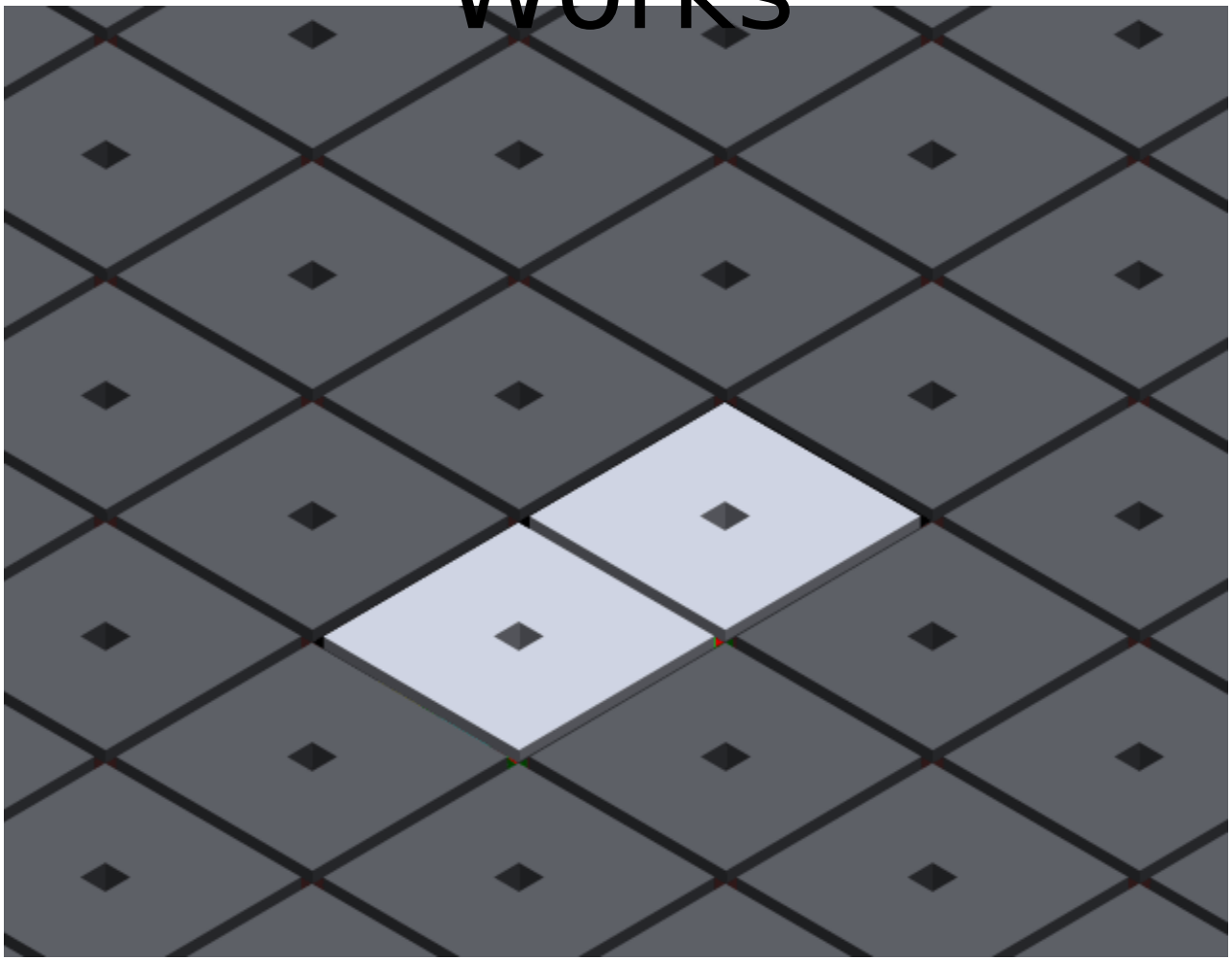

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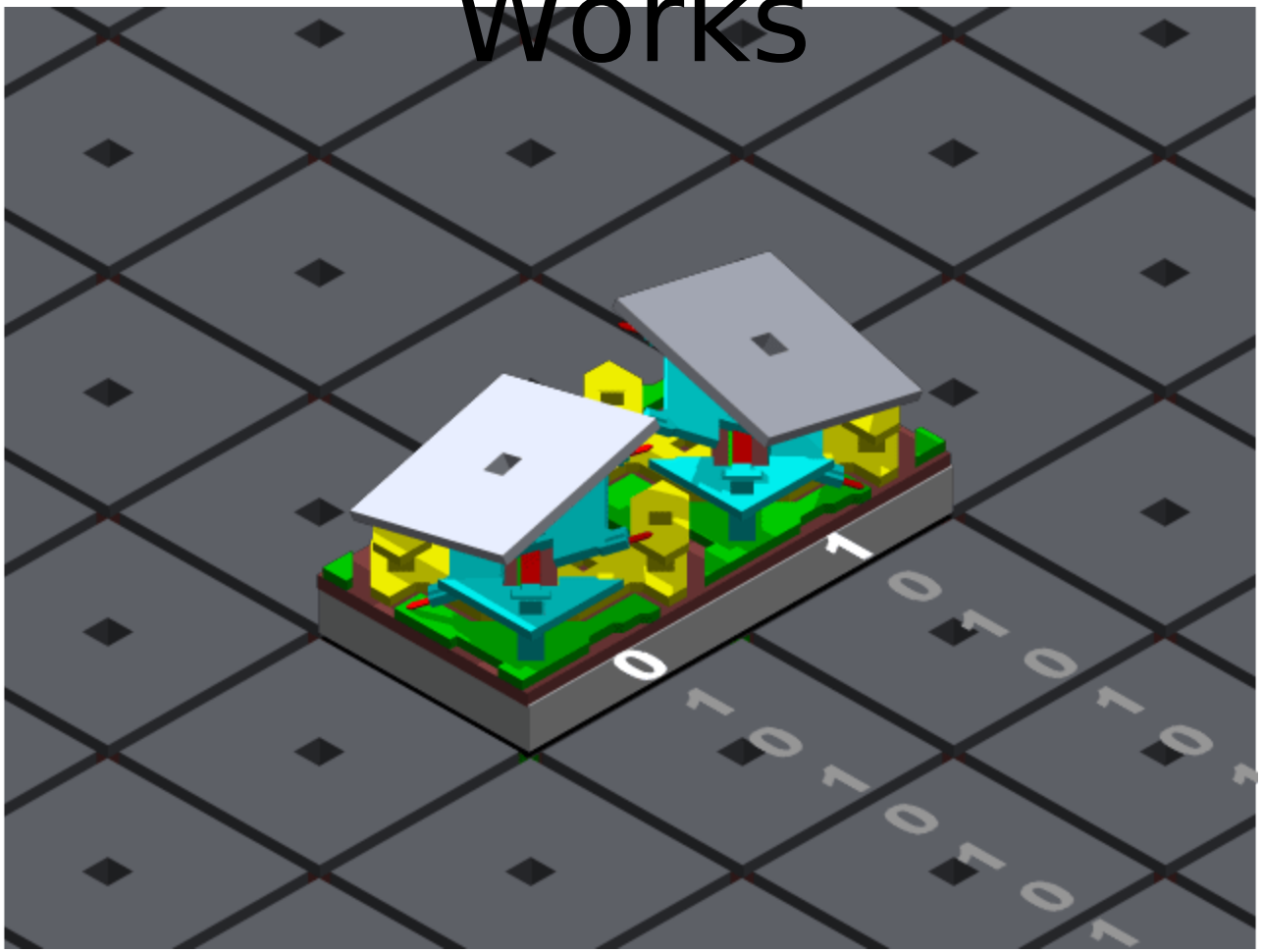

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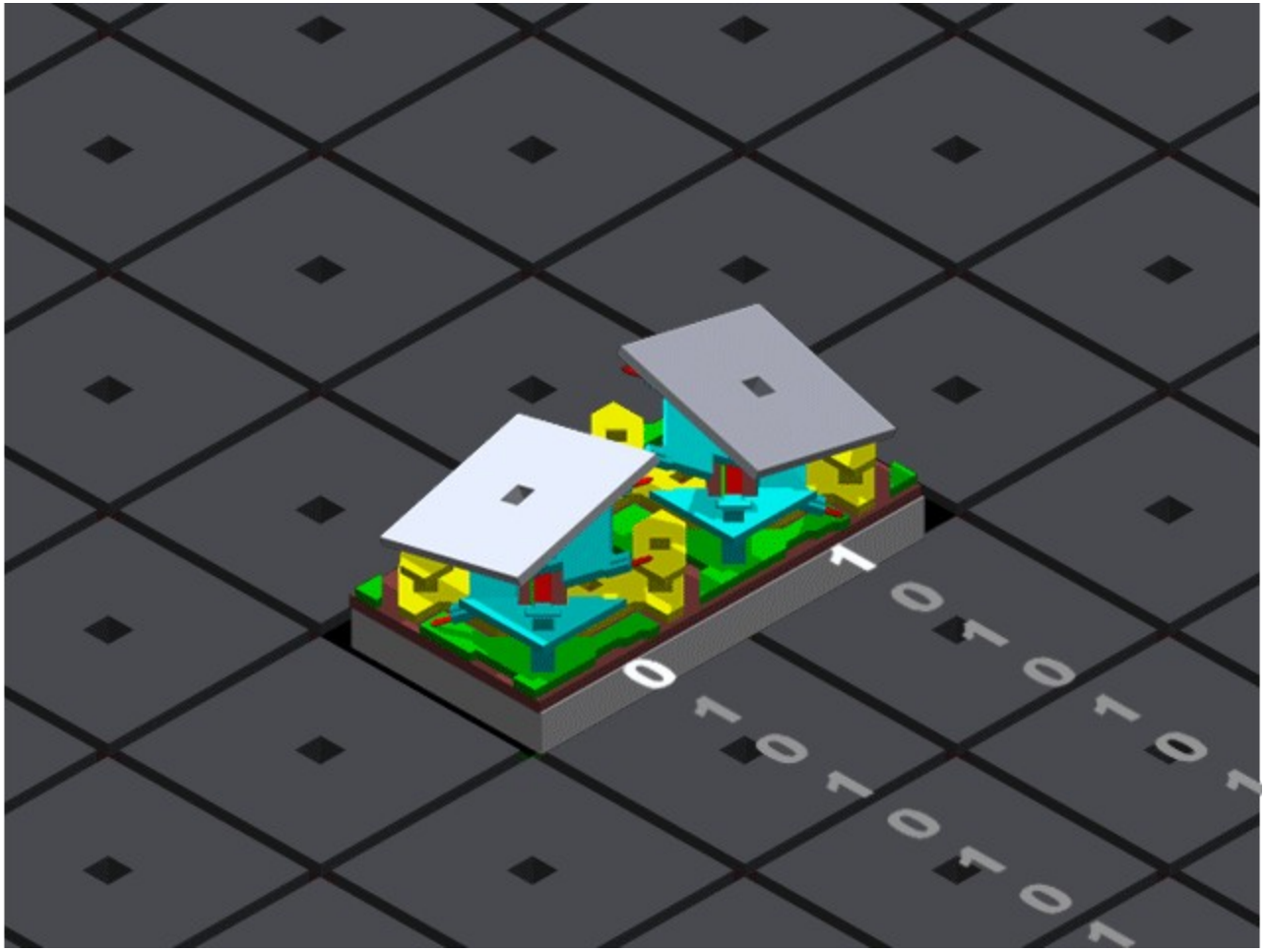

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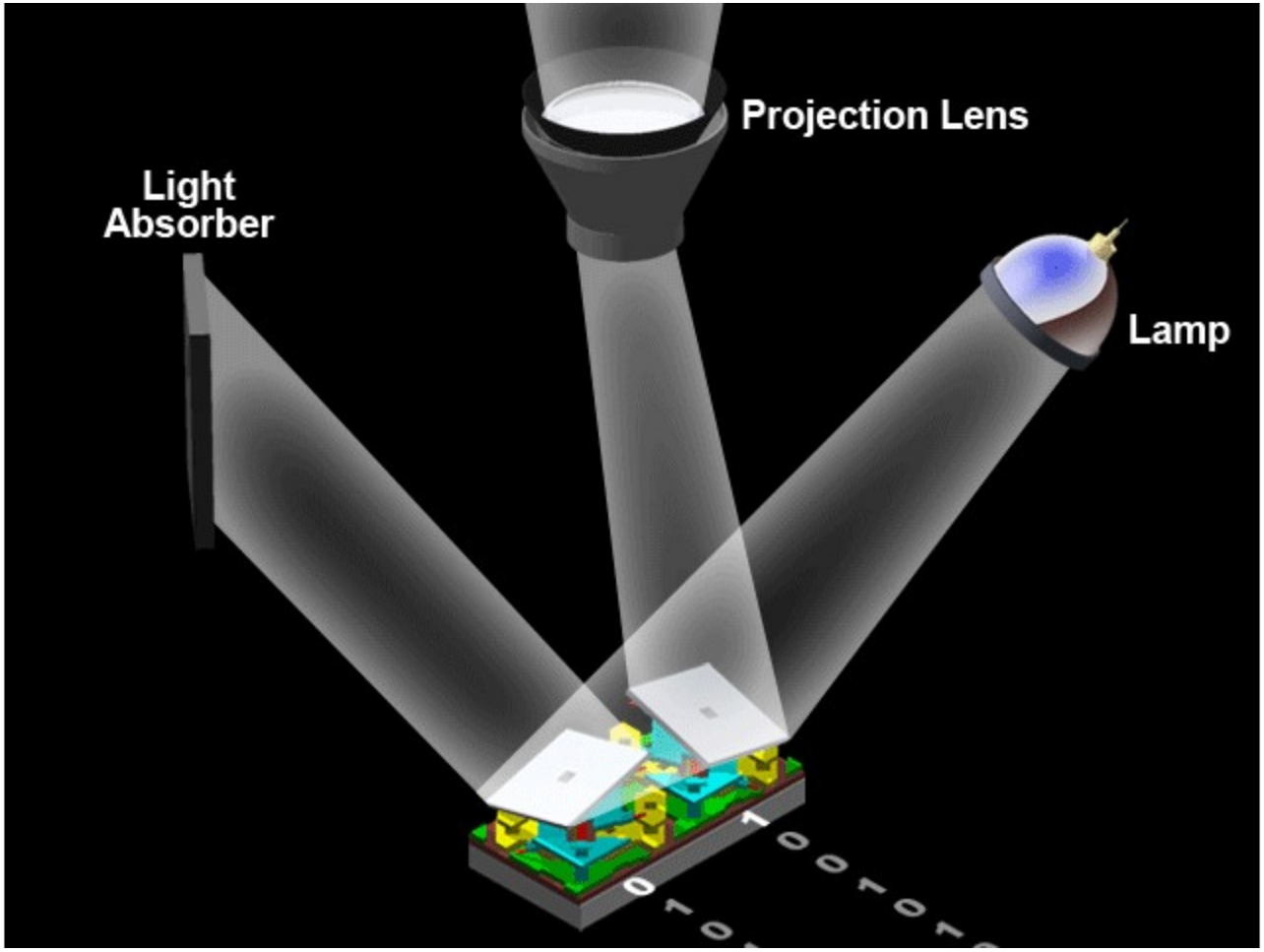

MEMS Integration

Today

- HDTV
- Front Projection Products
- Large Screen Movie Theaters

Tomorrow

- Projection displays for cell phones and PDAs
- 3D imaging for medical

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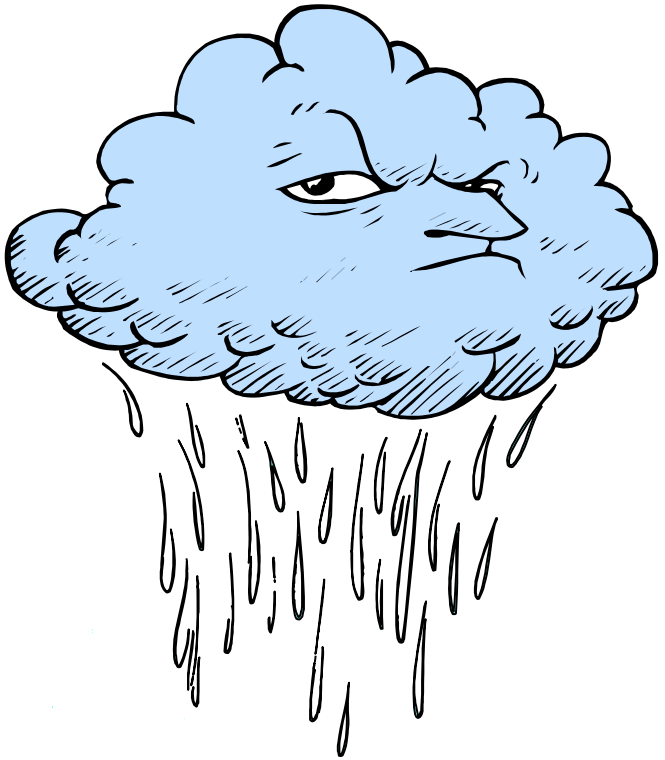
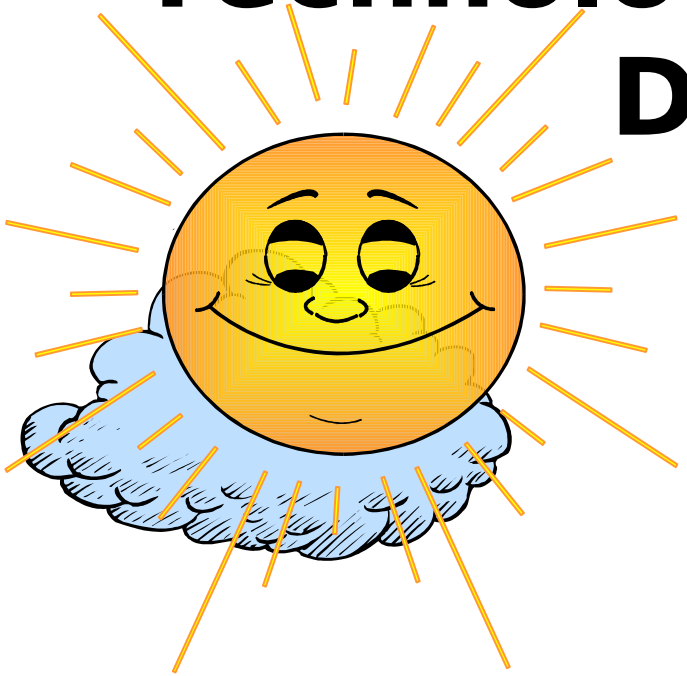
Technology in the Next Decade



Moore’s Law is predicted to stagnate toward the end of the next decade …

Technology in the Next Decade



Moore's Law is predicted to stagnate toward the end of the next decade …

… but SOC Integration has the potential to continue IC cost reduction and to perpetuate growth of products for ubiquitous computing, perception & sensing.

Systems on Si